EXHIBIT B -Pg 1

APPELLANTS' BRIEF ON APPEAL

DOCKET NO.: SC11931TP
APPLICANT: Thomas S. Kobayashi et al.
FILED: February 14, 2002
SERIAL NO. 10/075,218
DATE MAILED: March 5, 2004

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED IN THE MAIL PACKAGE

1.	x	Return Postal Card
2.	x	1 page Transmittal Form
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TRANSMITTAL FORM		
	Application Number	10/075,218
	Filing Date	February 14, 2002
	First Named Inventor	Thomas S. Kobayashi
	Group Art Unit	2814
	Examiner Name	Dana Farahani
Total Number of Pages in this Submission	Attorney Docket Number	SC11931TP

ENCLOSURES (check all that apply)

- [X] Fee Transmittal Form
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- [ ] Amendment/Reply
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- [ ] Affidavits/Declaration(s)
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- [ ] Response to Missing Parts/ Incomplete Application
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- [ ] Assignment Papers (for an Application)
- [ ] Drawing(s)
- [ ] Licensing-Related papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation, Change of Correspondence Address
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Remarks

- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter with appropriate copies
- [ ] Other Enclosure(s) (please identify below)
  - [ ] Response to Restriction Requirement
  - [ ] Associate Power of Attorney
  - [ ] RCE

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	Kim-Marie Vo	Registration No.	50,714
Signature	Kim-Marie Vo		
Date	March 5, 2004		

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage thereon, as first-class mail, in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313 or facsimile transmitted on the date listed below:

Typed or printed name	Elaine Cox		
Signature	Elaine Cox	Date	3/5/04

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FEE TRANSMITTAL

Patent fees are subject to annual revision

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330

Complete if Known

Application Number	10/075,218
Filing Date	February 14, 2002
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Group Art Unit	2814
Attorney Docket No.	SC11931TP

METHOD OF PAYMENT (check all that apply)

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☒ Deposit Account:

Deposit Account Number: 502117

Deposit Account Name: Motorola, Inc.

The Director is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fees(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)		Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	780	2004	365	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

		Previously Paid**		Extra Claims		Fee from below		Fee Paid
Total Claims		- 20	=		X	18	=	
Independent Claims		- 3	=		X	86	=	
Multiple Dependent						280	=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	* Reissue independent claims over original patent
1205	18	2205	9	*Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late Provisional filing	
1053	130	1053	130	Non-English specification	
1812	2520	1812	2520	For filing a request for ex parte Reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1480	2254	740	Extension for reply within fourth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1510	1451	1510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1330	2453	665	Petition to revive – unintentional	
1501	1330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of IDS	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

SUBTOTAL (3) ($) 330

* Reduced by Basic Filing Fee Paid

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Kim-Marie Vo	Registration No.	50,714
Signature	Kim-Marie Vo	Telephone	(512) 996-6839
		Date	March 5, 2004

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In re Application of:
Thomas Kobayashi, et al.
Serial No.: 10/075,218
Filed: February 14, 2002
For: SEMICONDUCTOR DEVICE HAVING A FUSE AND METHOD OF FORMING THEREOF

March 5, 2004

Art Unit: 2814
Examiner: D. Farahani
Docket No.: SC11931TP

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS ALEXANDRIA, VA 22313, ON: 3/5/04
MOTOROLA, INC.
Elaine Cox
SIGNATURE
DATE 3/5/04

APPELLANTS' BRIEF ON APPEAL

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313

BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed pursuant to 37 C.F.R. §1.192 in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent. Please charge the filing fee of $330.00 (37 C.F.R. §1.17(f)) to Deposit Account 502117. This page is enclosed in triplicate for this purpose.

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REAL PARTY IN INTEREST

The present application is wholly assigned to MOTOROLA, INC., a Delaware corporation with its headquarters in Schaumburg, Illinois.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Appellants originally filed claims 1-20 of the present application on February 14, 2002. In an Office Action mailed May 30, 2002, the Examiner rejected claims 1-4, 8-14 and 17-20 under 35. U.S.C. 102(e) over U.S. Patent 6,222,212 by Lee et al. ("Lee") and claims 5-7, 15 and 16 under 35 U.S.C. 103(a) over Lee. Appellants responded to the rejections in a communication faxed on August 26, 2002 by amending claims 1, 11 and 18 and canceling claims 10 and 19. In an Office Action mailed November 6, 2002 the Examiner maintained the rejections of the pending claims and made the rejection final. On January 2, 2003, Appellants submitted an amendment under 37 C.F.R. 1.116. The Examiner found that Appellants' arguments did not place the application in condition for allowance and mailed an advisory action stating so on January 21, 2003. On February 5, 2003, an Examiner Interview was held between the Examiner and the Appellants. No agreement was made. Appellants filed a request for continued examination, which was faxed on February 6, 2003. A preliminary amendment amending claims 1, 11 and 18 was faxed with the request for continued examination. In response to the preliminary amendment, the Examiner maintained the rejections of the pending claims, but did not make the rejection final, in an Office Action mailed May 19, 2003. Appellants responded by amending claims 1, 11 and 18 and adding new claims 21 and 22. This response was

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faxed on July 2, 2003. The Examiner responded with a final rejection mailed October 6, 2003. Appellants submitted an amendment under 37 C.F.R. 1.116 by facsimile on November 17, 2003. The Examiner responded with an advisory action mailed December 19, 2003. Appellants faxed a Notice of Appeal on January 6, 2004. This Appeal Brief is submitted in support of the Notice of Appeal.

STATUS OF AMENDMENTS

The claims being appealed are claims 1-9, 11-18 and 20-22. Claims 1, 11 and 18 were amended in communications mailed July 2, 2003, February 6, 2003, and August 26, 2002. Claims 21 and 22 were added in the communication mailed July 2, 2003. Claims 2-9, 12-17, and 20 are as originally filed.

SUMMARY OF THE INVENTION

Appellants' invention relates generally to semiconductor devices having fuses. Prior art fuses are often formed from metal lines, which are covered by a passivation layer. When it is desired to change the state of the electrically measured connection, portions of the fuse are removed in order to create an open. Typically, a portion of the fuse is physically severed (blown) by absorbing energy from a laser, breaking the passivation layer. When blowing through the passivation layer, any underlying dielectric or copper metal line, if present, will be exposed to the environment which decreases their material integrity.

Appellants' invention, more specifically, relates to a fuse, which can be selectively open-circuited, formed over a passivation layer and under packaging materials, such as an underfill and mold compound. This prevents the underlying dielectric layers and copper layers, if present, from degrading and also allows for lower power to be used when blowing through the fuse since the passivation layer doesn't need to be penetrated.

A discussion of one embodiment of the invention begins on page 7, about line 1, of the present application. Illustrated in FIG. 2, a

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semiconductor substrate (5) having a metal layer (45) is formed over a passivation layer (35). An optional barrier layer 40 may be present between the metal layer (45) and the passivation layer (35). The metal layer (45) and optional barrier layer (40), if present, may be patterned using a photoresist layer (50) to form the fuse (43), as shown in FIG. 3 and described on page 7, about lines 16-25. If desired, the fuse (43) can be blown, as shown in FIG. 4 and described at least on page 8, lines 10-12. Next the semiconductor device (5) including the fuse (43), either blown or unblown, is packaged as shown in FIG. 5 and described on page 9, about lines 3-8. A packaging material (55, 70) is formed over the fuse (43) as described on at least page 9, lines 9-10 and page 11, liens 15-18. Details of the processing and the rest of the device process are not necessary to understand the issues of the present appeal and therefore are not discussed further in this brief.

ISSUES

1) Are claims 1-4, 8, 9, 11-14, 17, 18 and 20-22 patentable over Lee (U.S. 6,222,212) in view of Fillion (U.S. 5,353,498) under 35 U.S.C. 102(e)?

2) Are claims 5-7, 15 and 16 patentable over Lee under 35 U.S.C. 103(a)?

GROUPING OF CLAIMS

The Appellants respectfully request that the appealed claims be considered according to the following division:

Group A: Claims 1-4, 8, 9, 11-14, 17, 18 and 20-22
Group B: Claim 7
Group C: Claims 5, 6, 15 and 16

The requested division is on the basis that the claims of Groups A and B are directed a semiconductor device having a packaging material formed over a

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fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill, but Group A is rejected over Lee in view of Fillion under 35 U.S.C. 102(e) and Group B is rejected over Lee only under 35 U.S.C. 103(a). The claims of Group C are directed to a fuse comprising metal nitride and are rejected over Lee under 35 U.S.C. 103(a). Appellants submit that the claims of each group stand or fall together.

ARGUMENTS

Arguments for Group A

A reference is anticipatory if it discloses all limitations of a claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. du Pont*; 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); *American Hospital Supply v. Travenol Labs*, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984). Appellants respectfully submit that Lee and Fillion, alone or together, fail to disclose all limitations of the claims of Group A. More specifically, with respect to independent claims 1, 11 and 18, Lee and Fillion, alone or together, fail to teach (or suggest) "a packaging material [formed] over the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill." (See lines 6-8 of claim 1, lines 14-16 of claim 11 and lines 7-9 of claim 18 in the Appendix.) For a claim to be anticipated, "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPW2d 1051, 1053 (Fed. Cir. 1987). However, using more than one reference for an anticipation rejection has been held proper in three circumstances: **(i)** to show the primary reference contains an "enabled disclosure" (*In re Samour*, 571 F.2d 559, 197 USPQ 1 (CCPA 1978 and *In re Donohue* 766 F.2d 531, 226 USPQ 619 (Fed. Cir. 1985).; **(ii)** to show an inherent characteristic of the primary reference (*Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749)(Fed. Cir. 1991); and **(iii)** to show the meaning of a term used in the primary reference (*In re Baxter Travenol Labs.*, 952 F.2d 388, 21 USPQ2d 1281 (Fed. Cir. 1991).

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As a first point, the Examiner's rejection does not fall under one of the three exceptions listed above and for this reason the rejection is improper. The Examiner contends, "Lee does not disclose the packaging material is a mold", "Fillion discloses ...a substrate 24 that is made of [a *sic*] mold material...," and "[t]herefore, [i]t would have been within the level of ordinary skill in the art to use a mold material as the substrate 806 due to versatileness of the material...." Pages 2-3 of the final Office Action mailed on October 6, 2003. Thus, the Examiner is alleging that one of skill in the art would be motivated to substitute Fillion's alleged mold material for Lee's alleged packaging material. Combining the teachings or suggestions is not suitable for an anticipatory rejection and instead is an obviousness rejection. "If it is necessary to reach beyond the boundaries of a single reference to provide missing disclosure of the claimed invention, the proper ground is not §102 anticipation, but §103 obviousness." *Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1577 (Fed. Cir. 1991). Therefore, for at least this reason the anticipation rejection of the claims in Group A is improper.

Secondly, even if the Examiner applied the two patents so that the application of the two references falls within one of the exceptions to an anticipation rejection so that more than one reference can be used, the anticipation rejection is still improper. Of the three situations, only the last one, to explain the meaning of a term used in the primary reference, is possible based on the rejection. Lee is the primary reference, and, in theory, the Examiner could attempt to use Fillion to explain the meaning of "substrate" used in Lee. However, the use of Fillion to explain the meaning of the phrase "substrate" in Lee is improper. When read as a whole, as required by *W.L. Gore &Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984), all of the substrates discussed in Lee are semiconductor substrates. (Since all substrate are the same in Lee and the Examiner relies on Lee's substrate 806, in the discussion when a particular example is used, Appellants will refer to Lee's substrate 806.) As described in the background section of Lee, Lee is trying to solve the problem of incompatibility and processing complexity of forming programmable devices on the same semiconductor substrate as conventional logic elements, for example, using conventional processing. (See column 1, line 53 – column 2, lines 15.) Lee defines conventional

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processing as being formed on wafers. (Column 4, lines 26-36.) Wafers are known to be semiconductor materials or substrates. See Mayer and Lau, Electronic Materials Science: Integrated Circuits in Si and GaAs, pgs. 15-16, New York, 1990. Lee's solution involves forming programmable devices on one semiconductor substrate, forming other devices, such as logic devices, on another semiconductor substrate and joining them together. (See column 5, lines 1-4 and column 11, lines 52-54.)

Lee describes that substrate 705 in FIG. 7 is a semiconductor substrate. (Column 11, lines 14). FIGS. 8A and 8B, which include element 806, are "different embodiments for providing bonding pad connections" than that shown in FIG. 7. (Column 12, lines 1-3). By inference, the substrates in FIGS. 8A and 8B are therefore the same materials as that described in FIG. 7 and thus the substrate 806 is a semiconductor substrate. This is further supported by the fact that Lee states, "Programmable element 813 can be any of the programmable elements previously described." (Column 12, lines 11-12). The programmable elements are previously described with regard to FIG. 7 in column 11, lines 19-20. In order for the programmable element 813 to be any programmable element previous described the substrate 806 must be any substrate previously described and hence, is a semiconductor substrate.

While Appellants agree that the broad term "substrate" taken alone and without context could be a semiconductor substrate, a packaging material substrate, or another type of substrate, all references in Lee are to a semiconductor substrate due to the context in which "substrate" is used. Just because Lee fails to repeat the entire phrase "semiconductor substrate" and instead sometimes uses the shorthand "substrate" does not mean that Lee teaches that the substrate can be any substrate, such as a packaging material. Lee needs to be taken as a whole and for at least the above reasons when viewed as a whole every substrate in Lee is a semiconductor substrate. It is improper for the Examiner to pick and choose from the prior art. *In re Antonie*, 559 F.2d 618, 620, 195 USPQ 6, 8 (CCPA 1977). ("[I]t is this invention *as a whole*, and not some part of it, which must be obvious under 35 USC 103".)

The Examiner contends, "A packaging material, interpreted in in [*sic*] its broadest sense, could as well be a semiconductor material, that is a semiconductor package." Advisory Action mailed on December 19, 2003.

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Regardless as the truth of this statement, the statement is irrelevant to the issue. The issue is not whether a packaging material can be a semiconductor material and instead, the issue is whether Lee's semiconductor (substrate) material can be a packaging material. The Examiner is arguing the converse of the issue at bay. Even if a packaging material can be a semiconductor material, it bears no truth on the issue of whether a semiconductor material can be a packaging material. To show that proving the converse of a statement does not prove the statement, Appellants will give a example from geometry. While a square is a rectangle, a rectangle is not a square. As almost every adult knows, a square has four equal sides and four ninety-degree angles. Although a rectangle also has four ninety-degree angles, it has two sets of sides that are equal in length to each other. Therefore, proving that a square is rectangle, does not prove that a rectangle is a square and in fact, a rectangle is not a square. Applying this to the current issue, the Examiner needs to focus on showing that Lee's semiconductor (substrate) material can be a packaging material, not that a packaging material can be a semiconductor material. Thus, Examiner's assertion of the latter in response to Appellants arguments after final rejection, is irrelevant even if true. Appellants do not discuss the truth of the statement herein as it is not an issue and is beyond the scope of the rejection.

Lee only describes that the substrates are semiconductor substrates, not packaging material substrates. A packaging material substrate is not a subclass of semiconductor substrate because packaging materials, such as underfills or molds as stated in independent claims 1, 11 and 18, are not semiconductors (e.g., silicon). In addition, Lee teaches away from the substrates being packaging material substrates, because Lee teaches that FIG. 2B is an unpackaged integrated circuit and all subsequent processing of FIG. 2B fails to teach or suggest forming packaging processes and using a packaging material substrate.

The Examiner relies on Fillion to show that Lee's substrate can be a packaging material. However, for reasons discussed above, Lee's substrate is a semiconductor substrate. Thus, Lee properly defines what substrate is being discussed therein and thus the use of Fillion to explain the meaning of "substrate" is unnecessary. The Examiner is using Fillion as extrinsic evidence to explain (or as Appellants discuss below to expand, which is improper) a term used in Lee. Extrinsic evident can be used if it is "clear

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that the missing descriptive matter is necessarily present in the thing described in the reference and that it would be so recognized by persons of ordinary skill." *Continental Can Co. USA, Inc. v. Mondanto Co.*, 948 F.2d 1264, 1267-68 (Fed. Cir. 1991) citing *In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981). However, there is no missing descriptive matter in Lee. Lee fully explains that the substrate is a semiconductor substrate and therefore the use of any extrinsic evidence is not needed to explain what Lee means by the phrase "substrate," and therefore, no extrinsic evidence should be used. For at least this reason the use of Fillion as extrinsic evidence is improper.

A third reason the rejection is improper is that the Examiner is using Lee to expand and not to explain Less' substrate. Using a second reference to expand the meaning of a word in a first reference is an improper use of a second reference under an anticipation rejection. See *In re Baxter Travenol Labs.*, 952 F.2d 388, 21 USPQ2d 1281 (Fed. Cir. 1991). The Examiner is taking the use of the term "substrate" in Lee and expanding it beyond the meaning of a semiconductor substrate to a packaging substrate. As discussed above, a semiconductor substrate does not include a packaging substrate, such as an underfill or a mold.

Furthermore, even if the Examiner had made an obviousness rejection instead of an anticipation rejection, the claims of Group A are still patentable over Lee and Fillion. Even if the Examiner could replace Lee's substrate with Fillion's substrate under an obviousness rejection such a combination would destroy the functionality of Lee. Lee's substrate cannot be replaced with Fillion's packaging material substrate because it would destroy the functionality of Lee because Lee requires the substrate 806 to be a semiconductor substrate capable of having a programmable element formed within it using conventional semiconductor processes (See Column 1, lines 53-67 and Column 2, lines 29-60.) A packaging material, such as a mold, as taught in Fillion is not a semiconductor substrate and cannot be used as a substrate to form a programmable element using conventional semiconductor processing. Fillion teaches a list of material that could be a packaging material and none of the material are semiconductors. (Column 5, lines 59-Column 6, lines 29), especially as taught by Fillion as being packaging materials. In other words, no where does Fillion teach or suggest using a semiconductor material as a packaging material.

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Arguments Common to Groups B and C

The Examiner rejects Groups B and C under 35 U.S.C. 103(a) over Lee. Appellants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness, which is the burden of the USPTO when rejecting claims under 35 U.S.C. 103. *In re Reuter*, 651 F.2d 751, 210 USPQ 249 (CCPA 1981). The case of prima facie obviousness is not met because the reference cited by the Examiner in support of the rejection does not teach all of the claim limitations. *In re Royka*, 180 USPQ 580 (CCPA 1974); *In re Wilson*, 165 USPQ 494 (CCPA 1970); *In re Fine*, 5 USPQ2d 1596 (CAFC1988). More specifically, Lee fails to teach or suggest "a packaging material formed over the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill." (See lines 6-8 of claim 1 and lines 14-16 of claim 11 in the Appendix.)

As a first point, Lee fails to teach or suggest a substrate that is a mold compound. Lee describes in FIG. 7 that substrate 705 is a semiconductor substrate. FIGS. 8A and 8B, which include element 806, are "different embodiments for providing bonding pad connections" than that shown in FIG. 7. (Column 12, lines 1-3.) By inference, the substrates in FIGS. 8A and 8B are therefore the same materials as that described in FIG. 7 and thus the substrate 806 is a semiconductor substrate. This is further supported by the fact that Lee states, "Programmable element 813 can be any of the programmable elements previously described." (Column 12, lines 11-12.) The programmable elements are previously described with regard to FIG. 7 in column 11, lines 19-20. In order for the programmable element 813 to be any programmable element previous described the substrate 806 must be any substrate previously described and hence, is a semiconductor substrate.

All references in Lee to a "substrate" are to a semiconductor substrate. Just because Lee fails to repeat the entire phrase "semiconductor substrate" and instead sometimes uses the shorthand "substrate" does not mean that Lee teaches that the substrate can be any substrate, such as a packaging material. Lee needs to be taken as whole and for at least the above reasons when viewed as a whole every substrate in Lee is a semiconductor substrate. It is improper for the Examiner to pick and choose from the prior art. *In re Antonie*.

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Lee only describes that the substrates are semiconductor substrates, not packaging material substrates. In addition, Lee teaches away from the substrates being a packaging material substrates, because Lee teaches that FIG. 2B is an unpackaged integrated circuit and all subsequent processing of FIG. 2B fails to teach or suggest forming packaging processes and using a packaging material substrate.

Furthermore, claims 7 depends from claim 1, which is rejected over Lee and Fillion. Appellants submit that the Examiner should have rejected claim 7 over Lee and Fillion because if Lee and Fillion are needed to reject claim 1 at least the same references are needed to reject a claim that depends from claim 1. However, even if the Examiner rejected claims of Groups B and C over Lee in view of Fillion, the combination would also fail to teach or suggest a substrate that is a mold compound because the combination of Lee and Fillion destroys the functionality of Lee as described above with respect to the claims of Group A. Therefore, for at least these reasons, the claims of Groups B and C are patentable over Lee under 35 U.S.C. 103(a).

Arguments for Group C

The Examiner rejects Group C over Lee under 35 U.S.C. 103(a). Appellants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness, which is the burden of the USPTO when rejecting claims under 35 U.S.C. 103. *In re Reuter*, 651 F.2d 751, 210 USPQ 249 (CCPA 1981). The case of prima facie obviousness is not met because the reference cited by the Examiner in support of the rejection does not teach all of the claim limitations. *In re Royka*, 180 USPQ 580 (CCPA 1974); *In re Wilson*, 165 USPQ 494 (CCPA 1970); *In re Fine*, 5 USPQ2d 1596 (CAFC1988). More specifically, Lee fails to teach or suggest fuse comprising a metal nitride. (See lines 1-2 of claims 5, 6, 15 and 16 in the Appendix.)

The Examiner acknowledges that Lee fails to teach or suggest a fuse comprising metal nitride. The Examiner contends, "it would have been within the level of ordinary skill in the art to use metal nitride instead of metal oxide [for the fuse] because of its superior adhesive properties" and refers to column 5, lines 43-44 of Lee for support. In column 5, lines 43-44, Lee does not mention metal nitride or provide support that a superior

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adhesive property is desirable for a fuse. Even if Lee did teach that a superior adhesive property is desirable for a fuse, the Examiner fails to provide any support that a metal nitride has this property. Therefore, the Examiner fails to provide support that a metal nitride has good adhesive properties and fails to provide motivation to look for a material with good adhesive properties. All claim limitations must be taught or suggested in the prior art for a obviousness rejection. *In re Royka.* The Examiner is not providing prior art to teach or suggest all of the claim limitations of the claims of Group C. Therefore, the Examiner has not made a *prima facie* case of obviousness. For these reasons, the rejection of the claims of Group C over Lee is in error.

Respectfully submitted,

Kim-Marie Vo

Kim-Marie Vo
Agent for Appellants
Reg. No. 54,714
Ph: (512) 996-6849

EXHIBIT B - Pg 16

APPENDIX

1. A semiconductor device, comprising:

a substrate having circuitry formed therein;

a passivation layer formed overlying at least a portion of the substrate;

a fuse, which may be selectively open-circuited, formed overlying the passivation layer; and

a packaging material formed over the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill.

2. A semiconductor device as in claim 1, wherein a recessed area is formed in the passivation layer and wherein at least a portion of the fuse is formed in the recessed area.

3. A semiconductor device as in claim 1, wherein the fuse comprises a metal.

4. A semiconductor device as in claim 3, wherein the fuse comprises aluminum.

5. A semiconductor device as in claim 1, wherein the fuse comprises a metal nitride.

6. A semiconductor device as in claim 1, wherein the fuse comprises a metal and a metal nitride.

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7. A semiconductor device as in claim 1, wherein the fuse comprises a metal having a thickness less than approximately 1 micron.

8. A semiconductor device as in claim 1, wherein the circuitry comprises a first circuit and a second circuit, the semiconductor device further comprising:

a first interconnect for electrically connecting the first circuit to a first portion of the fuse; and

a second interconnect for electrically connecting a second circuit to a second portion of the fuse,

wherein the first circuit and the second circuit are no longer electrically connected if the fuse is open-circuited.

9. A semiconductor device as in claim 1, wherein the fuse is electrically connected to only the circuitry, and is not electrically connected to anything external to the circuitry.

11. A semiconductor device, comprising:

a substrate having a first circuit formed therein and a second circuit formed therein, wherein the first circuit has a first contact area and the second circuit has a second contact area;

a passivation layer formed overlying at least a portion of the substrate;

a fuse, which may be selectively open-circuited, formed overlying the passivation layer, the fuse having a third contact area which is electrically coupled to the first contact area of the first circuit, and the fuse having a fourth contact area which is electrically coupled to the second contact area of the second circuit, wherein

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the first contact area of the first circuit and the second contact area of the second circuit are no longer electrically connected if the fuse is open-circuited; and

a packaging material formed over the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill.

12. A semiconductor device as in claim 11, wherein a recessed area is formed in the passivation layer and wherein at least a portion of the fuse is formed in the recessed area.

13. A semiconductor device as in claim 11, wherein the fuse comprises a metal.

14. A semiconductor device as in claim 13, wherein the fuse comprises aluminum.

15. A semiconductor device as in claim 11, wherein the fuse comprises a metal nitride.

16. A semiconductor device as in claim 11, wherein the fuse comprises a metal and a metal nitride.

17. A semiconductor device as in claim 11, wherein the first contact area of the first circuit and the second contact area of the second circuit are electrically connected only by way of the fuse.

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18. A method for forming a semiconductor device having a fuse, comprising:

providing a substrate;

forming a passivation layer overlying at least a portion of the substrate;

forming the fuse overlying the passivation layer; and

forming a packaging material over the fuse, wherein the packaging material is selected from the group consisting of a mold compound and an underfill.

20. A method of claim 18, further comprising:

blowing the fuse before forming a packaging material on the fuse.

21. A semiconductor device as in claim 1, wherein the packaging material is formed on the fuse.

22. A method of claim 18, further comprising:

forming the packaging material on the fuse.